



FIG. 2 PRIOR ART

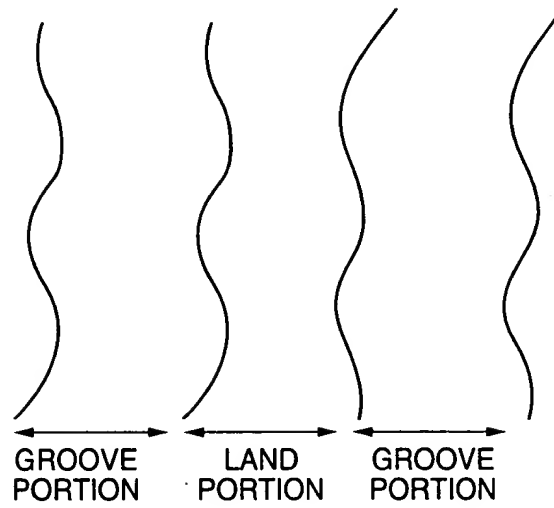


FIG. 3 PRIOR ART

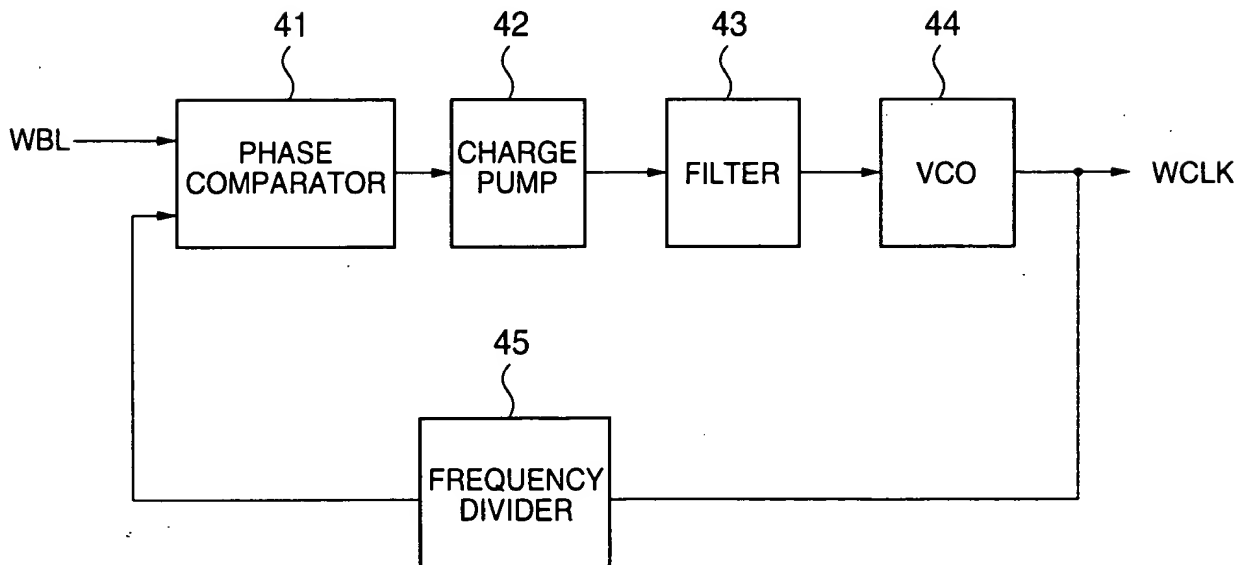


FIG. 4

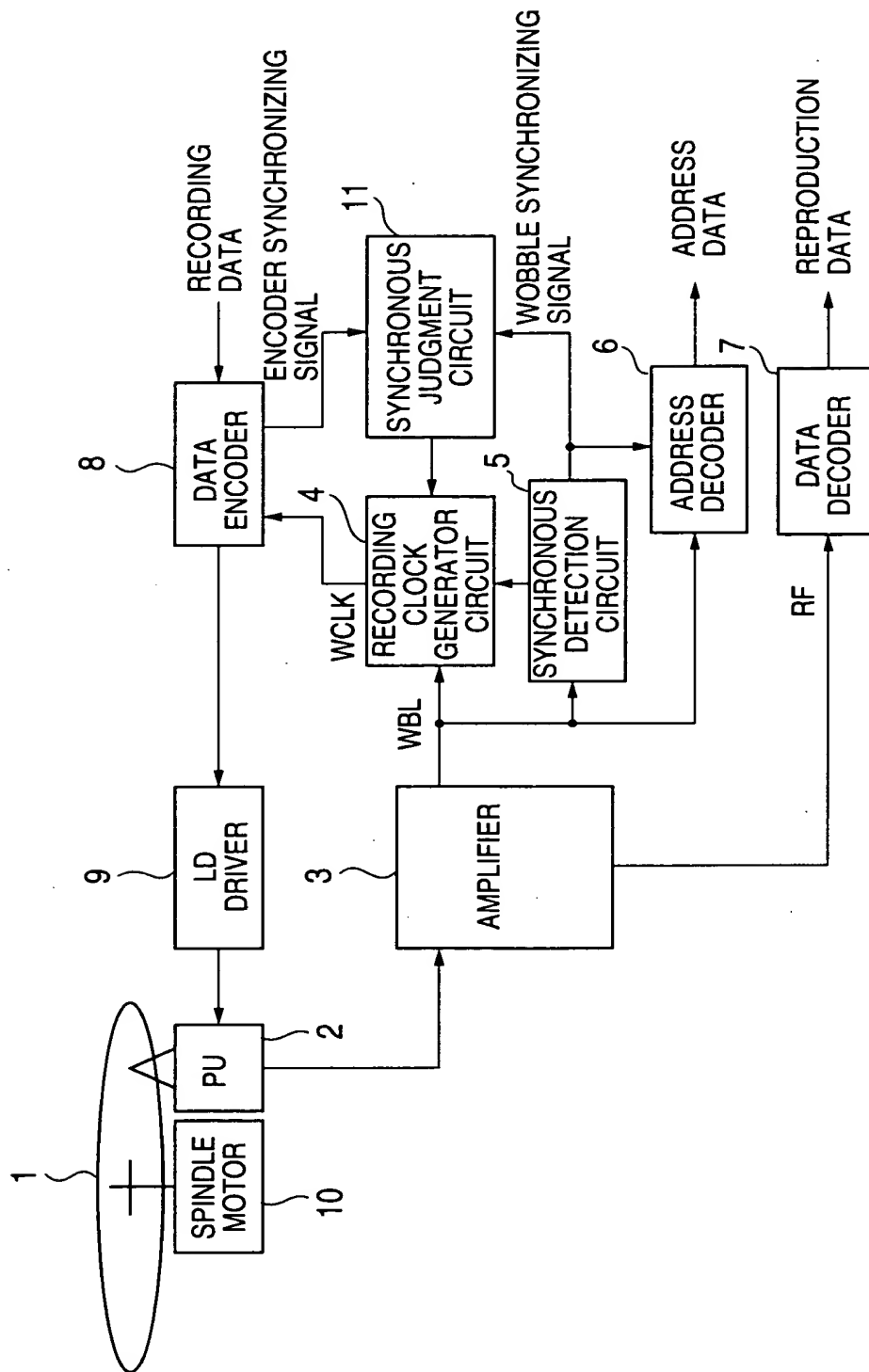


FIG. 5

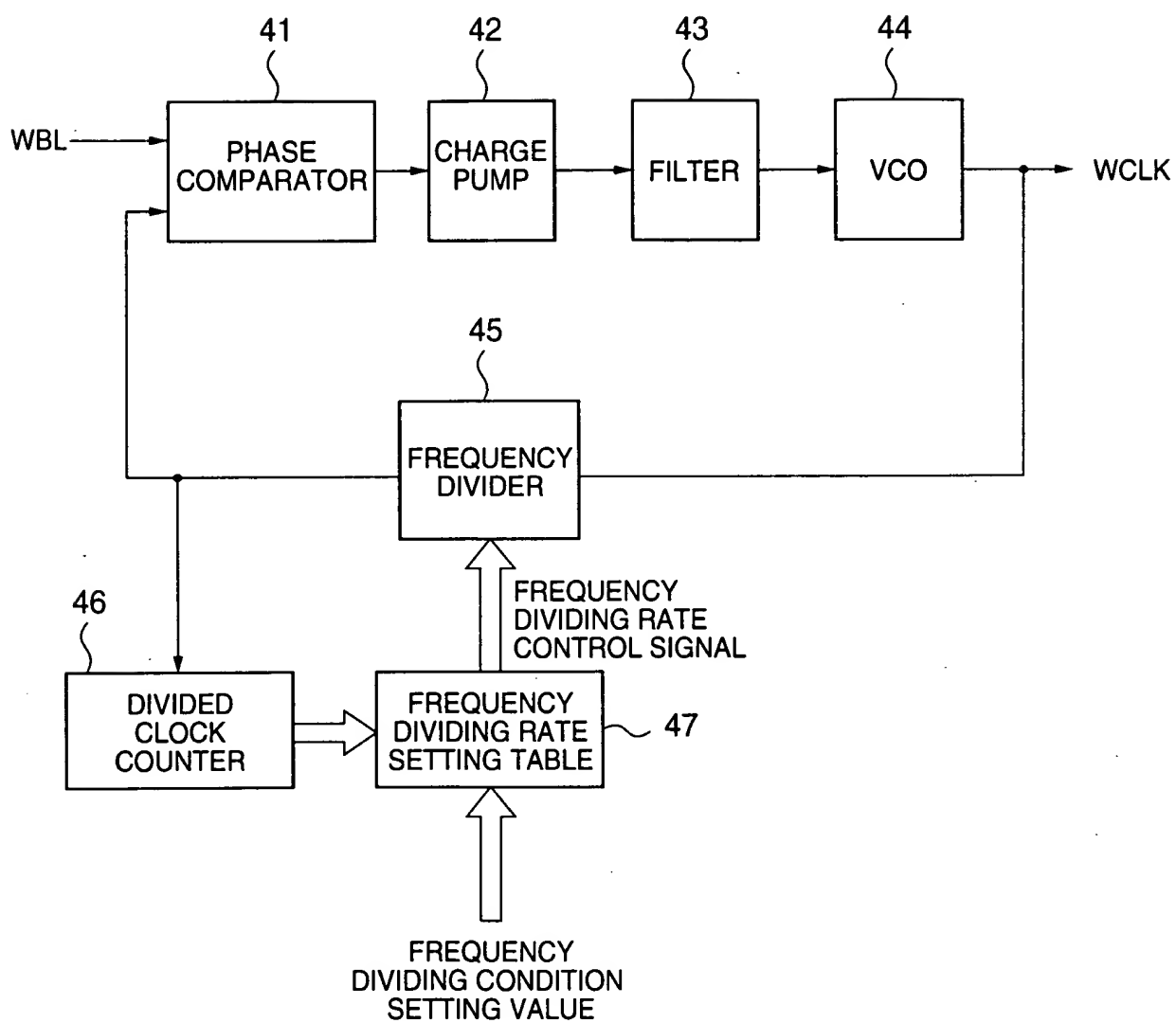


FIG. 7

FREQUENCY DIVIDING CONDITION SETTING VALUE	DIVIDED CLOCK COUNTER VALUE			
	0	1	2	3
0	ACNT	8 9 ... 15	8 9 10 ... 15	8 9 10 ... 15
	BCNT	0 1 ... 67	0 1 ... 67	0 1 ... 67
	SRFF			
1	ACNT	7 8 9 ... 15	8 9 10 ... 15	8 9 10 ... 15
	BCNT	0 1 ... 67	0 1 ... 67	0 1 ... 67
	SRFF			
2	ACNT	7 8 9 ... 15	7 16 17 ... 31	9 10 ... 15
	BCNT	0 1 ... 67	0 1 ... 67	0 1 ... 67
	SRFF			
3	ACNT	7 8 9 ... 15	8 9 10 ... 15	9 10 ... 15
	BCNT	0 1 ... 67	0 1 ... 67	0 1 ... 67
	SRFF			

FIG. 8A

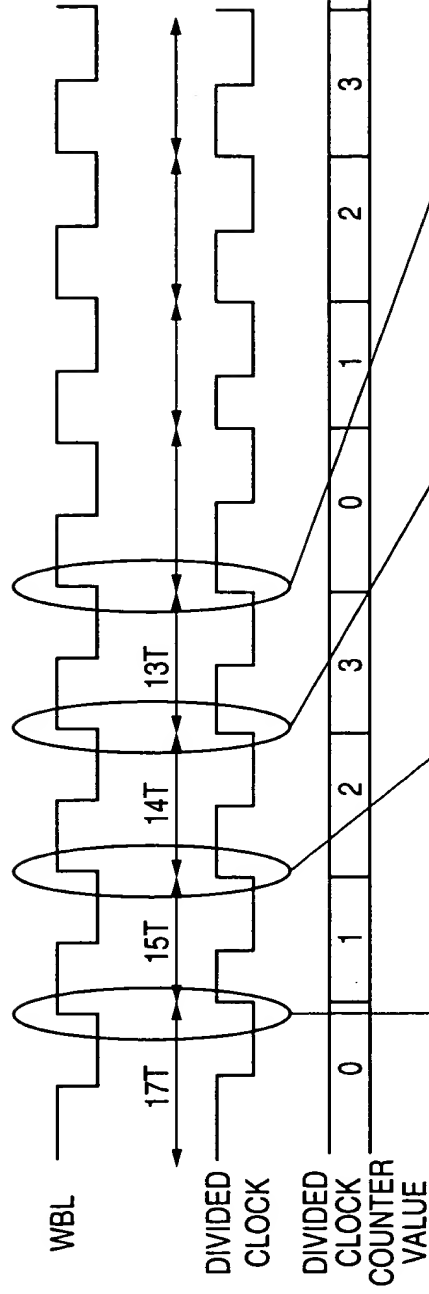


FIG. 8B

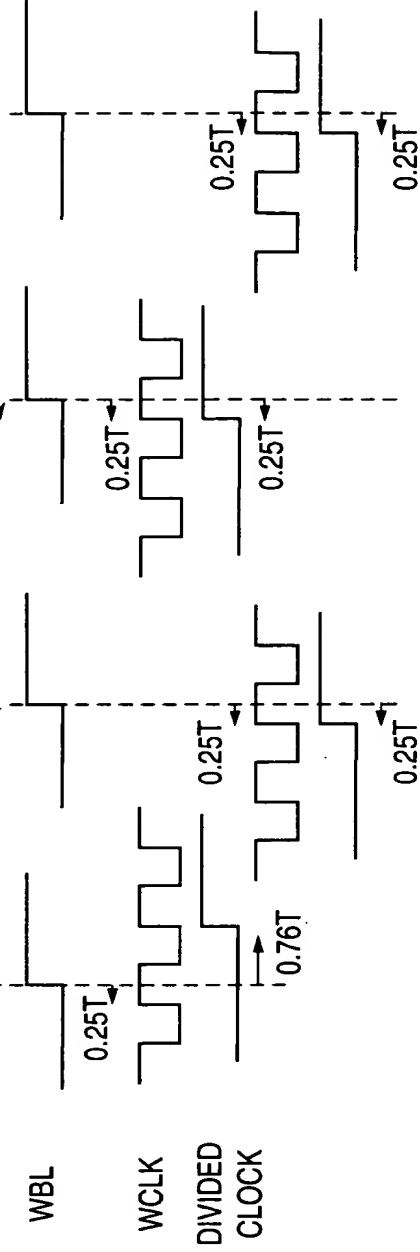


FIG. 8C

FIG. 8D

FIG. 8E

FIG. 8F

FIG. 8G

FIG. 9

FREQUENCY DIVIDING CONDITION SETTING VALUE	DIVIDED CLOCK COUNTER VALUE				
	3	0	1	2	3
A CNT	9 10 ... 15	7 8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15
3→0 BCNT	7	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7
SRFF					
A CNT	8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15	8 9 10 ... 15	9 10 ... 15
0→3 BCNT	7	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7	0 1 ... 6 7
SRFF					



FIG. 12

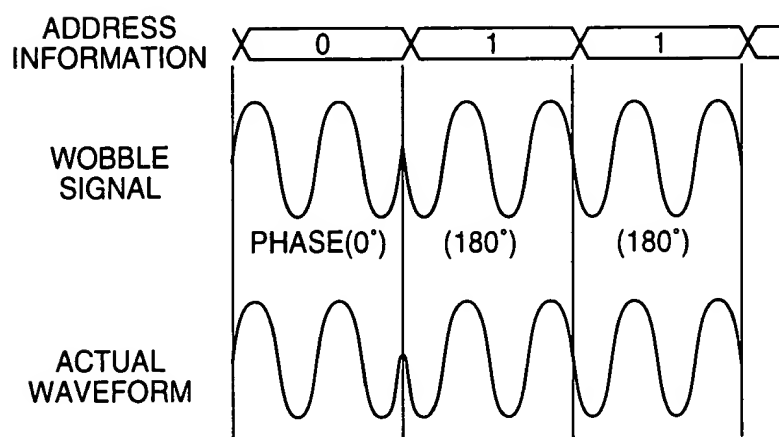


FIG. 13

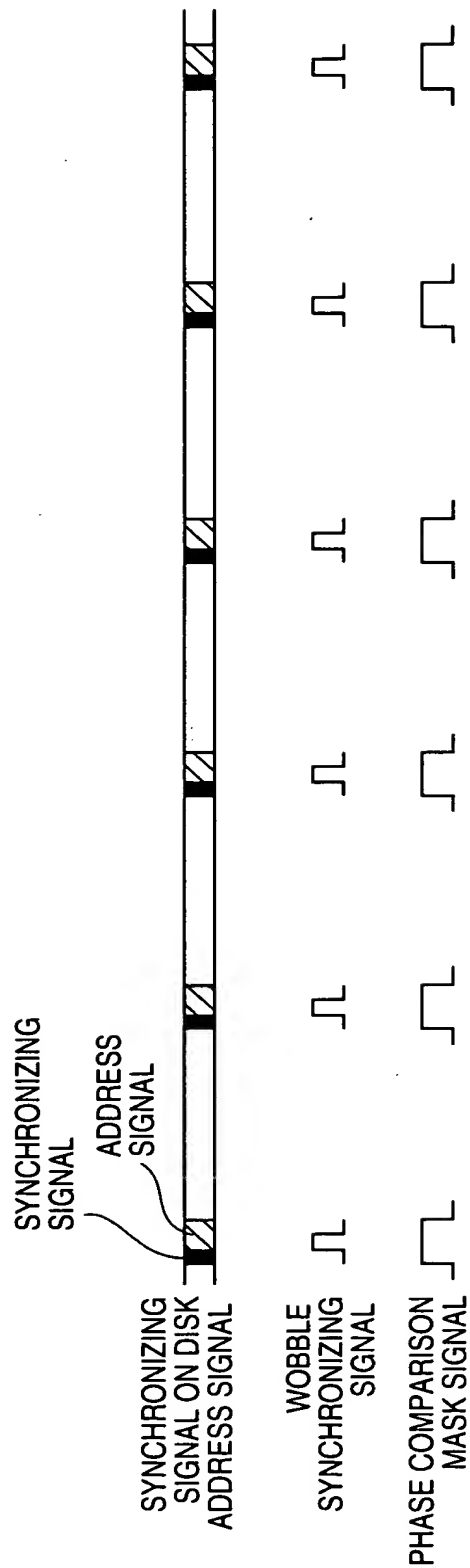


FIG. 14

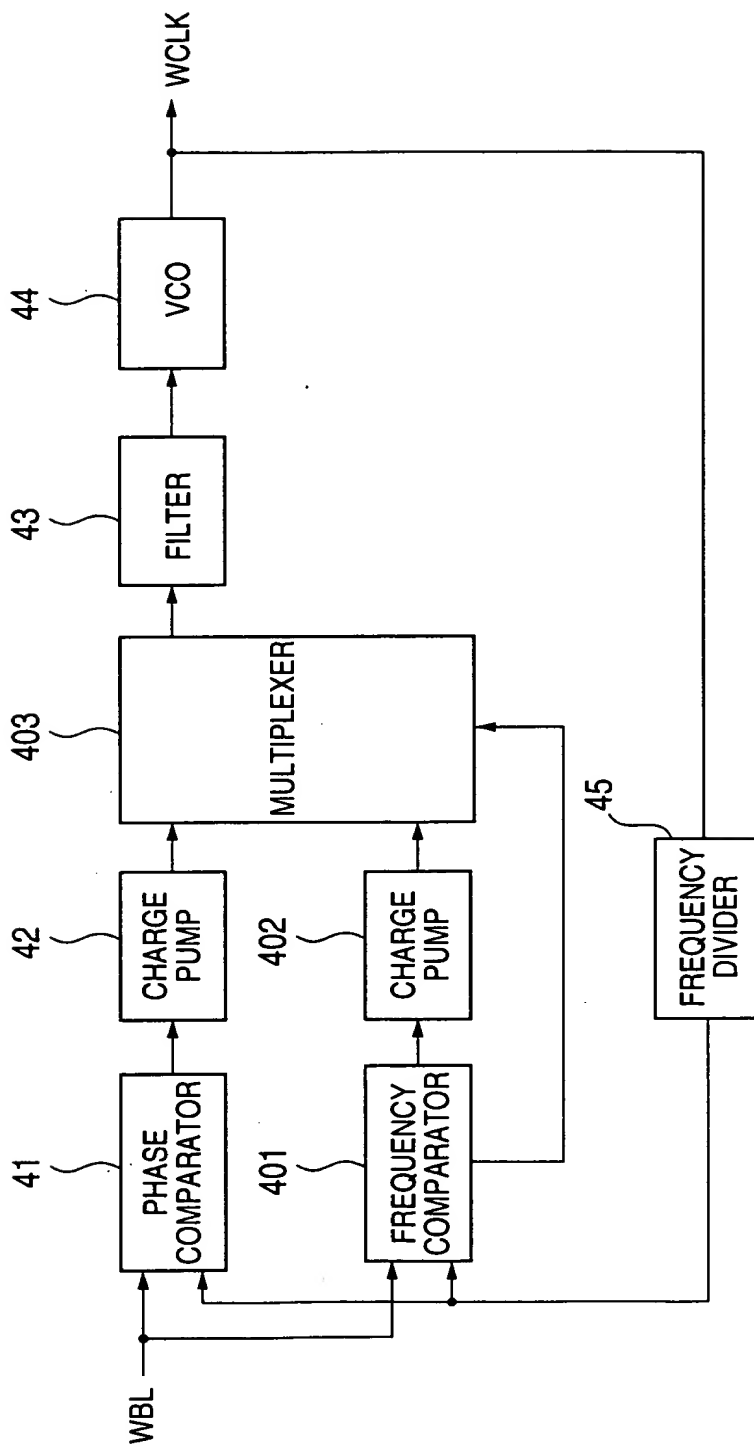


FIG. 15

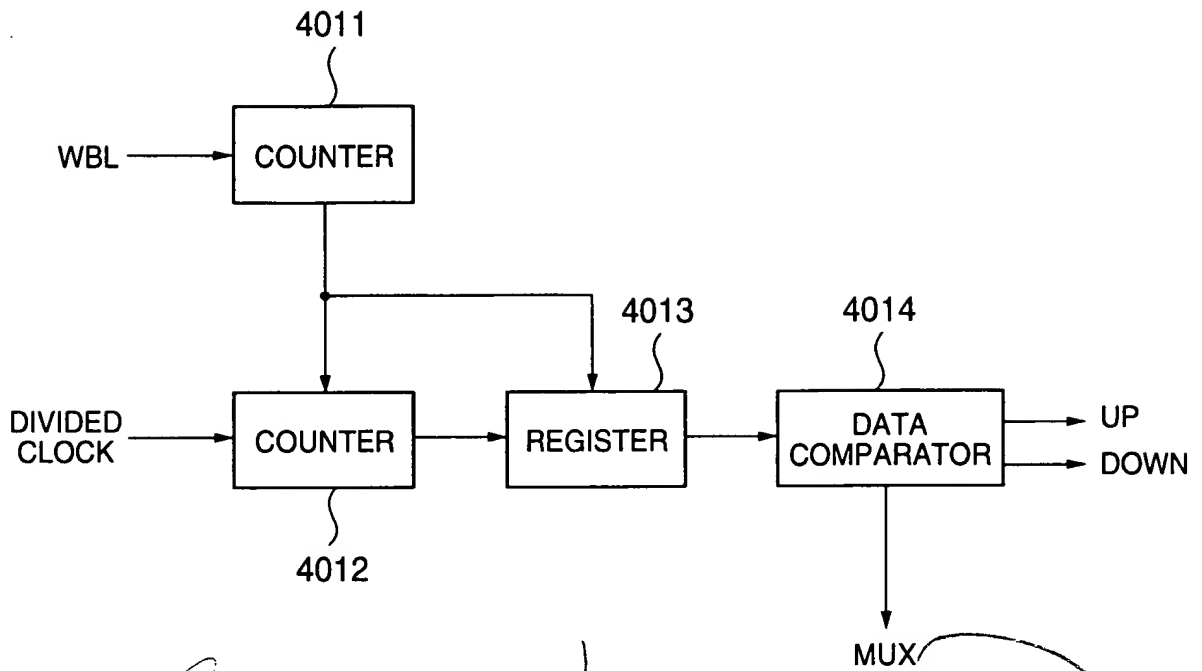


FIG. 16

